In the Claims:

Please amend the claims as indicated.

1. (Currently Amended) A method of accessing the testing means in a Field Programmable Gate Array ("FPGA") comprised of a plurality of functional groups ("FGs") comprising:

~~inputting~~inputting a function netlist defining a user circuit;

compiling said function netlist; and

generating a logic Built-In Self Test ("BIST") netlist;

wherein said BIST netlist replaces all user registers with scan registers with a scan chain routed as the physical silicon scan chains.

2. (Currently Amended) The method of claim 1 further comprising extracting scan chain from said logic BIST netlist and predicting an expected ~~syndrome~~ value.

3. (Currently Amended) The method of claim 2 further comprising applying said scan chain to the FPGA and obtaining actual ~~syndrome~~ values.

4. (Currently Amended) The method of claim 3 further comprising:

comparing said expected ~~syndrome~~ values with said actual ~~syndrome~~ values; and

flagging error if said expected values are different than said actual values.

5. (Currently Amended) A method of accessing the testing means in a FPGA comprised of a plurality of functional groups comprising:

~~inputting~~inputting a function netlist defining a user circuit;

optimizing said user circuit;

placing user cells into said FPGA functional unit;

defining routing structure to interconnect said functional units to implement said user circuit;

generating a programming bitstream;

programming said FPGA functional unit with said bitstream;

generating a BIST netlist, wherein said BIST netlist replaces all user registers with scan registers with a scan chain routed as the physical silicon scan chains;

extracting scan chain from said BIST netlist and predicting an expected ~~syndrome~~ value;

apply scan chain to FPGA and obtaining the actual ~~syndrome~~ values;

comparing said expected ~~syndrome~~ values with said actual ~~syndrome~~ values; and

flagging error if said expected values are different than said actual values.

6. (Currently Amended) An apparatus for accessing the testing resources in a programmed FPGA employing internal scan chains comprising:

means for generating a BIST netlist, wherein said BIST netlist replaces all user registers with scan registers with a scan chain routed as the physical silicon scan chains;

means for extracting a scan chain from said BIST netlist and predicting an expected ~~syndrome~~ value;

means for applying said scan chain to FPGA and obtaining actual ~~syndrome~~ values; and

means for comparing said expected ~~syndrome~~ values with said actual ~~syndrome~~ values.